**ABSTRACT:**

The vending machine is an automated machine that dispenses various products such as snacks, beverages, newspapers, tickets etc to customers when money or credit card is inserted. Vending machines are more accessible and practical than the convention purchasing method Now, vending machine market is a big business with huge annual revenue for leading nations like The USA, Japan, China and some other Asian countries including India. The paper aims to design a vending machine that can dispense three products of different prices with additional features of ‘return change’ when a coin of higher denomination is inserted and ‘return money’ when request is cancelled. The machine accepts coins of denominations five and ten. The finite state machine (FSM) approach is adopted for the design of vending machine. The design is achieved by formulating the Verilog code for the FSM- based machine using behavioural modeling and simulating the testbench for three products using Xilinx ISE tool.

**INTRODUCTION:**

Vending machines are automated systems designed to dispense items such as snacks, beverages, or tickets without the need for human intervention. These machines operate on embedded logic, where inputs such as coin denominations are used to initiate the delivery of goods. With the advancement of digital design methodologies, Hardware Description Languages (HDLs) like Verilog are increasingly being used to model such systems in a precise, scalable, and hardware-synthesizable manner.

In this project, a vending machine is designed using **Verilog HDL** to simulate the operation of a simple coin-based product dispenser. The system accepts ₹1 and ₹2 coins and is configured to dispense a product when the total amount reaches ₹5. The logic is implemented using a **Finite State Machine (FSM)**, where each state represents the total value accumulated so far. This approach makes the design intuitive and easy to scale or modify for additional features like change return or different item costs.

The use of Verilog HDL allows for efficient modeling, simulation, and synthesis of the design on FPGA platforms. Such designs are crucial for understanding the practical implementation of digital systems and their real-time behavior in embedded applications. The project also helps in reinforcing key concepts of sequential logic design, state machines, and modular HDL coding practices.

**Design Objective:**

To design a **coin-based vending machine** that:

* Accepts ₹1 and ₹2 coins.
* Dispenses a product when the total value reaches ₹5.
* Uses a **Finite State Machine (FSM)** to manage the sequence of operations.
* Is implemented using **Verilog HDL** for FPGA/ASIC applications.

**Design Approach: Finite State Machine (FSM)**

The vending machine is modeled using a **Mealy-type FSM**, where outputs depend on the current state and the current input. Each state represents the **total value of coins inserted** so far.

**State Transitions:**

Transitions occur based on the coin input:

* From S0, ₹1 → S1, ₹2 → S2
* From S2, ₹2 → S4; from S3, ₹2 → S5
* At S5, product is dispensed and FSM resets to S0

**Verilog Code**

module vending\_machine (

input clk,

input reset,

input [2:0] coin, // 3-bit input: 001 = ₹1, 010 = ₹2, 100 = ₹5

output reg product, // 1 = Product dispensed

output reg [3:0] change // Return change if inserted amount > ₹7

);

reg [3:0] total;

always @(posedge clk or posedge reset) begin

if (reset) begin

total <= 0;

product <= 0;

change <= 0;

end else begin

product <= 0;

change <= 0;

// Add coin value to total

case (coin)

3'b001: total <= total + 1; // ₹1

3'b010: total <= total + 2; // ₹2

3'b100: total <= total + 5; // ₹5

default: total <= total; // No coin

endcase

// Check if product should be dispensed

if (total >= 7) begin

product <= 1;

change <= total - 7;

total <= 0; // reset for next user

end

end

end

endmodule

**Testbench Code**

module test\_vending;

reg clk, reset;

reg [2:0] coin;

wire product;

wire [3:0] change;

vending\_machine vm (

.clk(clk),

.reset(reset),

.coin(coin),

.product(product),

.change(change)

);

// Clock generation

always #5 clk = ~clk;

initial begin

clk = 0;

reset = 1;

coin = 3'b000;

#10 reset = 0;

// Insert ₹2

#10 coin = 3'b010; // ₹2

#10 coin = 3'b000;

// Insert ₹5

#10 coin = 3'b100; // ₹5

#10 coin = 3'b000;

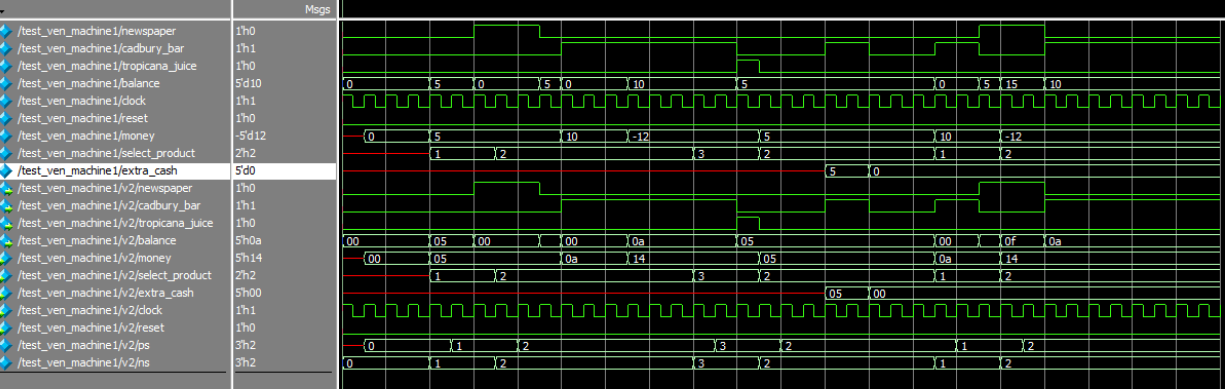
// Wait and observe

#50 $stop;

end

endmodule

**Output Waveform**

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**Conclusion**

In this project, a simple and efficient vending machine was successfully designed and implemented using Verilog HDL based on a Finite State Machine (FSM) approach. The system was modeled to accept ₹1 and ₹2 coins and dispense a product once the inserted amount reached ₹5 or more. The FSM design provided a clear and logical way to represent the sequential behavior of the vending machine, making it easy to manage state transitions and outputs.

The Verilog implementation demonstrated the practical application of digital design principles and HDL modeling techniques. Simulation results validated the correctness of the design, confirming accurate state transitions, proper product dispensing, and system reset functionality. This project illustrates how hardware description languages can be effectively used to create real-time digital systems suitable for synthesis on FPGA or ASIC platforms.

Overall, this vending machine project not only achieved its functional goals but also enhanced understanding of FSM design, Verilog coding, and digital system development, laying a strong foundation for more complex embedded system designs in the future.